Purpose of the Exam Preparation Guide

The intent of this guide is to set expectations about the content and the context of the exam and to help candidates prepare for the exam. In this guide, you will find recommended HP training courses, reference and study material to help you achieve a successful passing score.

Studies conducted by HP and Prometric show that a combination of course attendance and self-study maximizes the likelihood of passing the exam on the first attempt.

Audience

This exam is targeted for the following audience, with a minimum of three to five years’ experience on the NonStop S-Series platforms running the G-Series NonStop Kernel Operating System. Examples of job roles:

- Professional Services personnel who assist NonStop customers.
- Global Customer Support Center (GCSC) personnel, who may have specialized technical expertise in the operating system and NonStop applications and serve as support for both field support technicians and customers.
- Analyst SEs or Pre-Sales Technical Support (PSTS) personnel, who perform pre-sales consulting and technical account support.
- NonStop Technical Consultants (both internal and external), System Integrators and Consultant Partners, Authorized Service Channel Partners and Distributors, Customers authorized to service their own equipment.

General areas of content include: Process Life Cycle, Memory Management, Interrupts, and Data Structures, Message Systems, Guardian File System, I/O Subsystem, System Level and Hardware Considerations.

Certification Requirements

The NonStop Guardian Architecture Exam HP0-764 is an elective for certification as an Accredited System Engineer (ASE) in the HP NonStop S-series Systems track. It is also an elective for the HP NonStop Kernel Certified Systems Engineer (CSE) in the HP Operating System certification.
For further information on HP NonStop Systems track requirements, visit the website at

http://www.hp.com/go/certification

**Prerequisites**

None, but it is highly recommended that you have three to five years’ experience working in an HP NonStop Guardian environment.

**Exam Details**

The NonStop Guardian Architecture is a live exam. You will receive a score report with your results after testing is complete. You can use the report to identify areas of strength and learn about areas to improve, if necessary.

If you do not pass this exam, refer to your percentages for each core competency shown on your score sheet. Use these results to guide you in areas where you need to study or review more than other competencies.

**Test Information**

- **Number of test items:** 66
- **Item type:** multiple choice
- **Time commitment:** 90 minutes
- **Passing Score:** 34
- **Percent Correct:** 51%
- **Reference material:** No online or hard copy reference material will be allowed at the testing site.
Exam Content

The following outline represents the specific areas of content covered in the exam. Use this outline to guide your study and to check your readiness for the exam. The exam measures your understanding of these areas. The approximate percentage of exam questions dedicated to each major content area is included in parenthesis. Typically, the higher the percentage, the more questions will be on the exam.

1) Process Life Cycle (21%)

1.1 Describe what happens when processes are created

- Identify the system processes responsible for creating new processes
- Describe the role of these system processes
  - Describe what the Phoenix process is
- Demonstrate knowledge of a process control block (PCB) structure

1.2 Describe process termination

- Identify causes of process termination
- Describe how to obtain a SAVEABEND file
- Describe for what a SAVEABEND file is used
- List reasons for a process state to be "unstopable"

1.3 Demonstrate knowledge of the ready list mechanism

- Describe how a process is made active in a processor
- Describe how processes are normally merged to the ready list
- Describe how DP2 processes are merged to the ready list
- Describe how a process is prevented from monopolizing a processor

1.4 Describe how to obtain information on running processes

- Demonstrate knowledge about the information Peek displays on processes
- Demonstrate knowledge about the information Measure displays on processes
- Demonstrate knowledge about information TACL displays on processes
- Demonstrate knowledge of procedural interfaces to obtain information on running

1.5 Demonstrate knowledge of process states

- List the process states
- Describe process state transitions
- Demonstrate the role of a PCB in conjunction with semaphore mechanisms
1.6 Demonstrate knowledge of process security
- Describe the difference between PAID and CAID
- Describe the impact of licensing a program

1.7 Demonstrate knowledge of phandles and naming mechanisms
- Describe for what a process handle is used
- Describe different ways a process is named
- Describe the usage of process groups

1.8 Describe how wait/awake mechanisms are used
- Describe use of file_complete_ /awaitiox
- Identify the clients of the wait/awake mechanisms

1.9 Describe various logical segments of an executing process
- List logical segments created at process creation time
- Identify logical segments created dynamically
- Describe the use of the logical segments

1.10 Describe the environments in which processes execute
- Describe the TNS/R process environment
  - Describe the type of procedures a TNS/R process can call
- Describe the TNS process environment
- Describe the type of procedures a TNS process can call
- Describe the TNS accelerated process environment
- Describe how fixup is achieved for each environment during:
  - compilation
  - link editing
  - loading

1.11 Describe how shared code is used
- Describe the differences between shared code and linking procedures
- List examples of shared run-time library (SRL) usage
- Describe mechanism for accessing SRLs

1.12 Describe the function of process pairs
- Describe the use of active backup vs passive backup
- Describe the checkpoint mechanism

2) Memory Management (17%)

2.1 Describe virtual-to-physical memory mapping
- Describe the virtual memory mapping mechanism
- Describe different views of virtual memory (kuseg, kseg*)

2.2 Demonstrate knowledge of memory management implementation
- Describe the purpose of level-1 and level-2 cache
- Describe how code spaces are shared
- Describe how flat segments are shared
- Describe how priv mode relates to virtual memory

2.3 Demonstrate knowledge of logical and physical tables
- Describe some of the common tables used in memory management
- Explain the use of the segment page table
- Describe the use of the process data space table (PDST)
- Describe the logical segment mapping procedure

2.4 Describe the use of logical segments
- Describe the different types of segments used in memory management
- Discuss limitations of logical segments
- Describe the attributes of logical segments
- Describe how logical segments are tracked

2.5 Demonstrate knowledge of the segment life cycle
- Explain how segments are allocated and de-allocated
- Explain how segments are resized

2.6 Describe the page faulting mechanism
- Explain when page faulting occurs
- Explain the difference between page swapping and page faulting

2.7 Demonstrate knowledge of the frame selection algorithm
- Describe the relevance of referenced and dirty bit
- Interpret memory related output from PEEK

2.8 Demonstrate knowledge of memory addressing
- Describe the difference between process-relative and processor-relative addressing
- Demonstrate knowledge of the address spaces
- Demonstrate knowledge of global data structures

2.9 Display knowledge of Kernel-managed swap facility (KMSF)
- Describe the use of KMSF reservations
- Explain the features of KMSF
- Interpret NSKCOM output
2.10 Demonstrate knowledge of tools used to monitor memory
   • Explain PEEK output as it relates to memory usage
   • Explain the use of MEASURE data to monitor memory usage
   • Describe how ASAP(X) output is used to monitor memory usage
   • Describe how GPA output is used to monitor memory usage

3) Interrupts (6%)
   3.1 Describe the interrupt life cycle
      • Define an interrupt
      • Describe how process control is returned to normal processing
      • Describe what happens when an interrupt occurs

   3.2 Define the interrupt environment
      • Describe how an interrupted process is notified
      • Describe the function of the system interrupt vector (SIV)

   3.3 Identify types of interrupts
      • Demonstrate knowledge of the dispatch interrupt
      • Demonstrate knowledge of the page fault interrupt
      • Demonstrate knowledge of the power failure interrupt
      • Demonstrate knowledge of the UCME interrupt

   3.4 Demonstrate knowledge of concurrent interrupt handling
      • Describe how some interrupts can be interrupted
      • Describe how some interrupts can be deferred
      • Identify interrupts that can not be deferred

4) Data Structures (11%)
   4.1 Describe how linked lists are used as a data structure
      • Demonstrate knowledge of the different types of linked lists
      • Describe the use of pointers within linked lists

   4.2 Describe the use of tables
      • Describe the format of tables
      • Demonstrate knowledge of how pointers are used within tables

   4.3 Demonstrate knowledge of how pools are used
      • Describe the format of pools
      • Demonstrate knowledge of how pools work

   4.4 Describe how contention controls are implemented
• Describe the mutual exclusion (MUTEX) mechanism
• Describe semaphore mechanisms

4.5 Describe how time management is implemented
• Describe the role of time list elements (TLEs) within time management
• Demonstrate knowledge of time synchronization
  o - between processors
  o - between systems

4.6 Describe the format of kernel data structures
• - DCT
• - MQC
• - SIV
• - PPL
• - NRL

5) Message Systems (12%)

5.1 Describe the client side of the message system
• Identify the differences between system and user processes
• Describe the information passed from the client to the message system
  o Define conditions where expedited data is used
  o Define requirements for server reply
• Describe the different message system data structures on the client side

5.2 Describe the server side of the message system
• Identify the differences between system and user processes
• Describe the information passed from the server to the message system
  o Define the data structure unique to the server side
  o Describe the implications of non-expedited data
• Describe the different message system data structures (server side)

5.3 Explain the different mechanisms for message transfer between processes
• Define where the information passed by the client is stored in the message system data structures
• Explain the differences between intra-processor, interprocessor and inter-node transfer

5.4 Identify the various messages used during interprocessor communication
• Describe the use of PIOs, such as the “I’m alive” message mechanism
• Explain the function of the global update protocol (GLUP)
5.5 List alternative mechanisms for communications between processes
   • Describe the function of the QIO subsystem
   • Describe the function of shared extended data segments

5.6 Explain network (Expand) file system extensions
   • Define the role of Expand line handler
   • Describe the effect of network considerations on the file system data structure(s)

6) Guardian File System (16%)

6.1 Identify key Guardian file system API procedures
   • Identify the key support services
   • Identify file system limitations

6.2 Describe file system data structures
   • Identify file system client side data structures
   • Identify file system server side data structures
     o System server
     o User server
   • Identify global file system data structures

6.3 Explain file system open considerations
   • Describe OPEN message considerations
     • Describe the usage of OPEN by system processes
     • Describe the usage of OPEN by application processes
       o High Pin process considerations
       o $Receive open considerations
     • Describe the effect of NOWAIT opens
   • Identify other file system messages
   • Identify considerations for syncdepth
     o Valid file types
     o Benefits
     o Limitations

6.4 Describe Guardian file system security
   • Identify file system type support
   • Describe file system limitations

6.5 Describe the features of the Enscribe file system extensions
   • Define the implication of partitioned files/alternate key files
   • Describe Enscribe Format 2 block structure
• Describe key-sequenced B-tree structure
• Describe an Enscribe key-sequenced block split

6.6 Explain the usage of DEFINEs
• Describe DEFINE creation:
  o Propagation
  o Post process creation
• Describe how Defines are accessed
• Describe the implication of using DEFINEs

6.7 Explain the usage of startup, assign and param mess
• Demonstrate knowledge of TACL conventions
• Describe where the values of startup, assign and param messages are kept

6.8 Demonstrate knowledge of Guardian disk file creation
• Describe the usage of the free space table (FST)
• Describe virtual disk support by SMF
• Describe disk file extent size and limitations

6.9 Describe support for Guardian disk I/O using cache
• Non-Enscribe disk file support
• Enscribe disk file support

7) I/O Subsystem (10%)

7.1 Demonstrate knowledge of ServerNet
• Describe the relationship between remote memory access (RMA) and ServerNet
• Describe the differences between ‘push’ and ‘pull’ mechanisms
• Explain the transfer mechanism for interprocessor
• Describe the role of the ServerNet address space in I/O operations
• Describe the format of ServerNet addresses
• Describe the ServerNet services layer

7.2 Demonstrate knowledge of communications I/O
• Describe the life cycle of a communications I/O
  o Identify how an I/O is initiated
  o Identify how the transfer occurs
  o Identify how the I/O completes
• Identify which components participate in a communications I/O operation
• Describe the driver layers
o Describe the data flow from application to device
- Explain the role of the SLSA subsystem

7.3 Demonstrate knowledge of storage I/O
- Identify which components participate in a storage I/O operation
  o Identify how an I/O is initiated
  o Identify how the transfer occurs
  o Identify how the I/O completes
- Describe the driver layers
- Describe the role of XIO
- Demonstrate understanding of the Bulk I/O architecture

7.4 Demonstrate knowledge of the WAN subsystem
- Identify how WAN devices are connected to the processor
- Identify the role of QIO within the WAN subsystem
- Identify how other I/O is implemented

7.5 Demonstrate knowledge of DP2 cache
- Describe the structure of cache configuration
- Explain the implications of cache hit vs miss for read and write
- Describe the mechanisms for displaying cache statistics
- Describe the relationship between cache and control points

7.6 Demonstrate knowledge of I/O subsystem management
- Identify what is specified and started as a result of sysgen
- Identify the components involved in configuring and starting devices dynamically
- Identify the components of subsystem management
  o Identify the role of I/O subsystem managers
  o Identify the role of the persistence manager
  o Identify the role of the storage IOP
  o Identify the role of the interrupt handler and module driver

8) System Load and Hardware Considerations (7%)

8.1 Demonstrate knowledge of the procedures involved in system cold load
- Describe how a processor loads the bootstrap
- Demonstrate knowledge of the bootstrap processes
- Demonstrate knowledge of the OSIMAGE
  o Describe relationship between CONFLIST and OSIMAGE
- Demonstrate knowledge of load-paths
- Demonstrate knowledge of the structures involved in cold-load
• Identify difference between processor load vs. system load

8.2 Demonstrate knowledge about the creation of non-sysgenned devices and generic processes
• Describe where configuration information is maintained
• Describe which processes are involved
• Demonstrate knowledge about STARTMODE attribute

8.3 Demonstrate knowledge of hardware implementation considerations
• Demonstrate knowledge of millicode function
• Demonstrate knowledge of floating point implementation

8.4 Demonstrate knowledge of system failure mechanisms
• Demonstrate knowledge about processor/system freeze mechanism
• Demonstrate knowledge about the processor halting mechanism
• Demonstrate knowledge of power fail ride-through
Recommended Training and Study References

This section lists training courses and documents that can help you acquire a majority of the knowledge and skills needed to pass the exam. You must also gain the practical experience outlined in this guide.

You are not required to take the courses listed in this section. However, HP strongly recommends that you attend the classes, participate in class labs, and thoroughly review all course material and documents before taking the exam, even if you believe you have sufficient on-the-job experience.

Instructor-Led Training

Use the information in this guide and the practical experience you have gained to determine your need for the HP instructor-led training.

The HP Certified Professional Program (Level 2) includes references to a variety of materials that provide information included on this certification exam. Completion of these HP courses and review of materials is recommended, but not required, for success on this exam.

Recommended Minimum Courses

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<th>Course Title</th>
<th>Part Number</th>
<th>Type</th>
<th>Length</th>
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<tbody>
<tr>
<td>NonStop Kernel Architecture</td>
<td>U4178S</td>
<td>ILT</td>
<td>8 days</td>
</tr>
<tr>
<td>NonStop Kernel Principles</td>
<td>U4179S</td>
<td>ILT</td>
<td>4 days</td>
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Additional Highly Recommended Courses

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<thead>
<tr>
<th>Course Title</th>
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</thead>
<tbody>
<tr>
<td>College courses pertaining to computer architecture, data structures and algorithms</td>
<td>ILT = Instructor-Led Training  ISP = Independent Study Program</td>
</tr>
</tbody>
</table>

Other Level 2 Recommended Resources

For all Level 2 NonStop ASE exams, it is highly recommended that the certification candidates be familiar with the contents of these two books (not available on NTL):

- **Performance Analysis of Transaction Processing Systems** by Dr. Wilbur Highleyman. This book can be downloaded from the NonStop website under the heading Current Exams and Preparation. Refer to the download link under the NonStop Performance Analysis and Tuning Exam Preparation Guide link.

  Note that this book is can be ordered from HP Publishing.

**Courses Descriptions**

Check web site course descriptions for prerequisites at:

http://www.hp.com/education/sections/nonstop.html

To register in HP NonStop courses, go to:

http://www.hp.com/cgi-bin/education/regform.cgi

You can also call 1 (800) 472-5277 in North America, to speak with an education consultant or register for courses. If you are in Canada, call 1 (800) 563-5089 or contact your local education and training resource. For other locations, refer to the HP certification web page for your geography and your regional or local contacts.

http://www.hp.com/go/certification

Or, you can send an email to nonstop.training@hp.com

**Additional Recommended Reference Materials for This Exam**

References for exam questions are found in the web-based HP NonStop Technical Library (NTL). The NTL can be accessed from these URLs:

Internal: http://techlibrary.cac.cpqcorp.net/ntl/

External: www.hp.com/go/ntl

Note that this exam preparation guide typically references the latest documentation release available at the time the exam was written.

**Documentation**

The information in this exam preparation guide is current as of release G06.18. However, you may find the information in earlier or later versions of the NonStop Technical Library (NTL) documentation as well. Information nested (~) indicates subsections emphasized in the document.

• COBOL85 for NonStop Himalaya Systems Manual (522555-001)
  ~ Compiler directives
  ~ SAVEABEND and NOSAVEABEND

• Enscribe Programmer’s Guide (520369-002)
  ~ Block Formats of Structured Files
    o Block Format for Structured Format 2 Files
  ~ General File Creation and Access Information
- Specifying the Appropriate Disk File ACCESSTYPE Parameter
  - Sequential Block Buffering
    - Specifying the Appropriate Disk File ACCESSTYPE Parameter
  - Key-Sequenced Files
    - Key-Sequenced Tree Structure
  - Unstructured Files Information
    - Creating Unstructured Files
    - Buffer Size

- Guardian Performance Analyzer Manual (135081)
  - Description of GPA Reports
    - Global Performance Indicators

- Guardian Procedure Calls (522629-003)
  - Guardian Procedure Calls (O)
    - OPEN Procedure
  - Guardian Procedure Calls (P)
    - Define Considerations
  - Guardian Procedure Calls (S)
    - SEGMENT_ALLOCATE_Procedure
    - SEGMENT_DEALLOCATE_Procedure
    - SEGMENT_USE_Procedure
  - J. System Limits

- Guardian Programmer's Guide (421922-001)
  - Creating and Managing Processes
    - Data Spaces for TNS/R Native Processes
  - Managing Memory
    - Sharing an Extended Data Segment
  - Managing Time
    - How the System Keeps Time
  - Synchronizing processes
    - Binary Semaphores
  - Using Floating Point Formats
  - Using DEFINEs
Using DEFINEs: An Example

Communicating with a TACL Process

Setting Up the Process Environment

Reading the Startup Sequence Without INITIALIZER

Guardian User’s Guide (425266-001)

Managing Users and Security

Interfaces for the Security Features

Performing Routine Disk Operations

Monitoring and Altering Swap Files

Kernel Managed Swap Facility Manual (425824-001)

Operator Messages for KMSF

214

Introduction

Kernel Managed Swap Process Flow

Managing Kernel Managed Swap Files

Stopping Swap Files

LAN Configuration and Management Manual (520469-003)

Overview of SLSA

Measure GUI User’s Guide (140772)

Monitoring Resource Use and Application Activity

Queuing for the CPU

NonStop Kernel Architecture, 05/30/02 (520554-001)

Mod 1, 1-9, 2-5, Mod 3, 1-34, 1-35, 3-17, 4-20, 4-16/17, 3-15, 4-32, 5-12, Lab 5, 6-3, 6-4, 6-10, 6-13, 6-14, 6-16, 6-21, 6-22, 6-23, 7-4, 7-18, 7-19, 7-20, 7-23, 7-25, 7-29, 7-31, 7-36, 7-40, 7-50, Mod 8, 8-5, 8-9, 8-14, 8-33, 8-34, 8-36, 8-37, 8-46, 8-65, 8-70, 8-76, 8-81, 9-3, 9-7, 9-8, 9-11, 9-15, 9-16, 9-18, 9-26, 9-27, 9-28, Mod 9-10, 10-5, 10-10, 10-12, 10-17, 10-25, 11-9, 11-15, 11-17, 11-22, 11-11

NonStop Kernel Principles (136913)

3-10, 3-16, 4-10, 5-8, 6-14, 6-27, 7-11, 7-16

NonStop S-Series FastPath Guide (525178-001)

System Description

NonStop S-Series System Configuration

NonStop S-Series Planning and Configuration Guide (523303-006)
Planning for System Availability and Support
  - Power Failure Functional Description

Nonstop S-Series Server Description Manual (520331-002)
  - Memory Addressing and Access
    - Selectable and Flat Logical Segments
    - Chart of Nonprivileged Space Allocation
    - Context Bound Addresses
  - Addressing in the Process Address Space
  - Interrupt System
    - Transferring Control to an Interrupt Handler
    - TNS Interrupts
    - Interrupt Masking
  - Instruction Processing Environments
  - Glossary
    - Kernel Subsystem Manager Process
    - SZZKRN

Input/Output Operations
  - Layers of I/O Components
  - I/O Process Models for Storage I/O

Nonstop Storage Management Foundation Users Guide (523562-002)
  - Introduction to Storage Management
  - SMF Architectural Concepts

PEEK Reference Manual (422607-001)
  - Peek Syntax and Examples
    - Elements of the Paging Display
    - Pool Elements
  - Glossary
    - NRL, PPL

SCF Reference Manual for the Storage Subsystem (523408-001)
  - Storage Subsystem Commands
    - FSTCACHING

System Generation Manual for G-Series RVU (523407-001)
~ Comparing SYSGENR for D-Series RVUs with SYSGENR for G-Series RVUs
  o Changes to the System Configuration Utilities

• QIO Configuration and Management Manual (424717-002)
  ~ Introduction to QIO

• TACL Reference Manual (429513-001)
  ~ Utils: TACL Commands and Functions
    o ACTIVATE Command
    o STATUS Command

• Viewsys User's Guide (103491)
  o ViewSys Overview

• WAN Subsystem Configuration and Management Manual (522463-003)
  ~ Overview of the WAN Subsystem
    o WAN Boot Process
    o Architecture and Components of the WAN Subsystem
    o Simple Network Management Protocol (SNMP) Trap Multiplexer
    o Process

Conclusion

HP wishes you success in the HP Certified Professional Program and in passing the exam for which you are preparing.