Integrity NonStop
Server Update:

July 20, 2006

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Nomi Trapnell, Product Manager, NS1000
NonStop Enterprise Division, HP
Agenda

• NS14000 Overview:
  – NSAA Architecture
  – Product Characteristics

• NS1000 Overview:
  – NSVA Architecture
  – Product Characteristics

• Architecture Availability Comparisons
• NonStop Server Roadmap
• Q/A
# NonStop server offerings

Common software across a choice of hardware configurations

<table>
<thead>
<tr>
<th>NonStop S-series family</th>
<th>HP Integrity NonStop server family</th>
</tr>
</thead>
<tbody>
<tr>
<td>NonStop software (with industry-standard APIs)</td>
<td></td>
</tr>
<tr>
<td>NonStop architecture</td>
<td></td>
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<tr>
<td>NonStop Advanced Architecture (NSAA)</td>
<td></td>
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<tr>
<td>NonStop Value Architecture (NSVA)</td>
<td></td>
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<tr>
<td>MIPS processor based</td>
<td></td>
</tr>
<tr>
<td>Intel Itanium 2 processor based</td>
<td></td>
</tr>
<tr>
<td>NonStop infrastructure</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>S88000 S78000 servers</th>
<th>NS16000 server Available today</th>
<th>NS14000 server Available today</th>
<th>NS1000 server Available today</th>
</tr>
</thead>
<tbody>
<tr>
<td>Available today</td>
<td></td>
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</table>

19 July 2006
Integrity NonStop server momentum

- 30% of our business from Integrity NonStop
- Over 250 partner solutions available
  - 90% of NonStop partners have Integrity NonStop solutions
- Deployed in every region and every major vertical

“We’re looking forward to being on the Itanium growth path.”
James Krause, managing director and CIO, Chicago Mercantile Exchange

“It’s important to keep the underlying microprocessor on an aggressive technology roadmap.”
Ron Cook, vice president of Technical Strategy & Operations, Radio Shack

“The Integrity NonStop server clearly takes NonStop systems performance to a new level.”
Helge Handen, WM-data Card Solutions manager

“We are very pleased that the NonStop server has moved to the industry-standard Intel Itanium 2 processor platform, with its aggressive technology roadmap and significant cost benefits.”
Richard Tims, CIO, Electronic Transaction Services Ltd.
HP Integrity NonStop Servers Architecture

- DMR: Dual Modular Redundancy
- TMR: Triple Modular Redundancy (Availability: seven 9’s)
- Itanium2 Servers in a cluster of uni-processors
- Loose Synchronization.
  - Each server runs on its own clock.
  - Each can perform soft error corrections without causing a mis-compare.
- Self-checked, shared-nothing transparent takeover
- Software fault tolerance
  - Message-based operating system
  - Process pairs
  - Transaction support
  - Distributed single-system image
- Fault-tolerant parallel database
- Application server transaction processing monitors

* = Logical synchronization units

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Integrity NonStop server delivers on the promise of outstanding value in its class

Infrastructure for the real-time enterprise

- Addresses most demanding transaction processing requirements
- Exploits industry standards
  - Itanium processor, Java, SQL, HP StorageWorks, HP OpenView
  - HP Systems Insight Manager
- Simple, flexible management
  - Single application image
  - OpenView
  - Virtualized resources
- Unique Innovation for continuous application availability
  - Integrated stack
  - Linear scalability up to 4,080 processors
  - Industry-leading data integrity

Driving down IT operating costs with infrastructure innovations

Lowest TCO*

<table>
<thead>
<tr>
<th>IBM zSeries (mainframe)</th>
<th>HP Integrity NonStop TMR</th>
<th>HP Integrity NonStop DMR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic cost</td>
<td>Application cost</td>
<td></td>
</tr>
</tbody>
</table>

* All figures in thousands of U.S. dollars.

Source: Standish Group, 2005
## Features at a glance

### NonStop Advanced Architecture (NSAA)

<table>
<thead>
<tr>
<th>NS16000 server</th>
<th>NS14000 server</th>
</tr>
</thead>
<tbody>
<tr>
<td>Availability up to seven 9s</td>
<td>Availability up to seven 9s</td>
</tr>
<tr>
<td>Software fault tolerance + DMR/TMR</td>
<td>Software fault tolerance + DMR/TMR</td>
</tr>
<tr>
<td>Fully scalable up to 4,080 processors (P-Switch in node + ServerNet internode); lowest latency</td>
<td>Scalable up to 2,040 processors (ServerNet internode)</td>
</tr>
<tr>
<td>Application Virtualization across nodes</td>
<td>Application Virtualization across nodes</td>
</tr>
<tr>
<td>Highest CPU power (1.6 GHz/6 MB cache)</td>
<td>~75% of NS16000 CPU (1.5 GHz/4 MB)</td>
</tr>
<tr>
<td>4, 8, or 16 GB main memory/CPU</td>
<td>4 or 8 GB main memory/CPU</td>
</tr>
<tr>
<td>2–16 CPU/node</td>
<td>2–8 CPU/system</td>
</tr>
<tr>
<td>NonStop hardware infrastructure</td>
<td>NonStop hardware infrastructure</td>
</tr>
<tr>
<td>Modular I/O; virtually unlimited connectivity plus NonStop S-series I/O (473 TB/node + XP + legacy devices)</td>
<td>Modular I/O; limited connectivity No NonStop S-series I/O (32 TB/node + XP + limited legacy)</td>
</tr>
</tbody>
</table>
Application Characterizations

- **Integrity NonStop NS16000**
  - Applications requiring significant central processing capability > 8 processors
  - Examples: Sabre OnLine Reservation, KDDI cellular SMS, large bank ATM switch with ACI Base-24, large hospital (>400 beds) supported by GE Centricity (nee IDX Carecast)

- **Integrity NonStop NS14000**
  - High availability applications with limited scalability
  - Examples: medium sized bank with Base-24, medium sized hospital (150 – 400 beds) for GE Centricity (nee IDX Carecast)
NSVA Architecture
Announcing the Integrity NonStop NS1000

Making NonStop more affordable

Industry standard hardware components + NonStop software advantages = NonStop Value Architecture (NSVA)
More choices: A portfolio of service levels

NonStop Advanced Architecture

NonStop Value Architecture

Integrity NonStop
High Availability Systems

Integrity NonStop 16000
Integrity NonStop 14000

Cost
Itanium® NonStop and the NonStop Value Architecture (NSVA)

NS16000/14000 4-processor system

NS1000 4-processor system

* = Logical synchronization units

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Itanium® NonStop and the NonStop Value Architecture (NSVA)

• Itanium2 Servers in a cluster of uni-processors
• 99.999% availability
• NSVA built on NonStop principles
  – Fault tolerant immediate "fail-fast" design paradigm
  – Error detection on all data paths, memory, and disk
  – Multiple paths to all data and communications
  – Hot-pluggable components
    • Online repair
    • Online addition/upgrade
• Software fault tolerance
  • Message-based operating system
  • Process pairs
  • Transaction support
  • Distributed single-system image
• Fault-tolerant parallel database
• Application server transaction processing monitors
HP Integrity NonStop NS1000

Most cost-effective, reliable, and easily managed software FT system

- HP rx2620 off the shelf
  - Intel Itanium 2 processor at 1.3 GHz with 3 MB cache
  - Supports 2, 4, 6, 8 processors
  - 4-8 GB memory per processor

- Software fault tolerance/fault isolation: same as other Integrity NonStop servers
  - NonStop OS; NonStop data base SQL/MX
  - Cluster programming transparency
  - Software I/O checksum

- Industry standard Fibre Channel and Ethernet connectivity
  - Supports Storage Area Network (SAN) & Internal Storage
  - Up to 32 TB storage per node (internal FC disks)
The NS1000: Brings significant TCO advantages to...

• Customers who have
  – High volume OLTP
  – High availability requirements
  – Medium to very high rates of data change

• Industry specific solutions
  – Small/med banking networks for ATM and point of sale (POS)
  – Hospitals with fewer than 150 beds (GE Centricity)
  – New application deployments in emerging countries
## NS1000 Configuration Options

- **2p, 4p, 6p, 8p Hardware base configurations (bundles)**
- **User can select additional Hardware from the price list e.g. data disks, etc.**
- **Upgrade Hardware bundles are also available in 2p increments**
- **Software is not bundled and is ordered from the NS1000 Software price list**
NS1000 – a winning cost model

Source: Standish Group, 2006

Identical ATM application workload running on Wintel, Sun and IBM;
NS1000 cost data provided to Standish group for primary research.
## HP Integrity NonStop server family

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<th>NonStop Advanced Architecture (NSAA)</th>
<th>NonStop Value Architecture (NSVA)</th>
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<td></td>
<td></td>
</tr>
<tr>
<td>Availability</td>
<td>Availability up to seven 9s</td>
<td>Availability up to five 9s</td>
</tr>
<tr>
<td>Software fault</td>
<td>Software fault tolerance + DMR/TMR</td>
<td>Software fault tolerance (N+1 CPU FT)</td>
</tr>
<tr>
<td>scalability</td>
<td>Fully scalable up to 4,080 processors (P-Switch in node + ServerNet internode); lowest latency</td>
<td>Scalable up to 8 processors with ServerNet (Expandable over Ethernet/ATM)</td>
</tr>
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<td>Application Virtualization across nodes</td>
<td>Application Virtualization across nodes</td>
<td>Application Virtualization across systems</td>
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<td>NonStop hardware infrastructure</td>
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<td>infrastructure</td>
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<td>Modular I/O; limited connectivity No NonStop S-series I/O (32 TB/node + XP + limited legacy)</td>
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NonStop Systems Performance Summary: Order Entry Benchmark

NonStop Systems Performance Summary

- S86000
- S88000
- NS1000
- NS14000
- NS16000

0 1 2 3

Series 1
NonStop Availability Comparisons:

- S-series
- NSAA
- NSVA
# Comparison against Fundamentals: NonStop Server Products

<table>
<thead>
<tr>
<th>Feature</th>
<th>S-Series 88K</th>
<th>NSAA DMR</th>
<th>TMR</th>
<th>NSVA NS1000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Redundant input power feeds</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Software fault tolerance</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>No single point of failure for a system</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>No single point of failure for a logical processor</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td><strong>Data integrity</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>End to end disk checksum</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Transactional consistency for clean failover</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Guaranteed Hardware Data Integrity</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td><strong>CPU Fault masking - application transparent</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transient faults</td>
<td>Good</td>
<td>Better</td>
<td>Best</td>
<td>Good</td>
</tr>
<tr>
<td>Hard faults</td>
<td>N</td>
<td>Yes</td>
<td>Yes!</td>
<td>N</td>
</tr>
<tr>
<td>Service error resilient</td>
<td>Good</td>
<td>Better</td>
<td>Best</td>
<td>Good</td>
</tr>
<tr>
<td><strong>SAN Fault Masking</strong></td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
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## Impact of CPU hardware faults

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<thead>
<tr>
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<th>NonStop S-series servers</th>
<th>NSVA</th>
<th>DMR</th>
<th>TMR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient fault</td>
<td>No impact</td>
<td>No impact</td>
<td>No impact</td>
<td>No impact</td>
</tr>
<tr>
<td>(particle-induced)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>main memory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transient fault</td>
<td>Lose logical CPU</td>
<td>Sometimes lose logical CPU</td>
<td>No impact</td>
<td>No impact</td>
</tr>
<tr>
<td>(particle-induced)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>other parts of the CPU</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intermittent fault</td>
<td>Sometimes lose logical CPU</td>
<td>Sometimes lose logical CPU</td>
<td>No impact</td>
<td>No impact</td>
</tr>
<tr>
<td>(underlying hardware defect)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hard fault</td>
<td>Lose logical CPU</td>
<td>Lose logical CPU</td>
<td>No impact</td>
<td>No impact</td>
</tr>
</tbody>
</table>

Note: Logical CPU failure invokes software takeover, system keeps running.
Cascading Faults

• Most outages result from cascading faults rather than single faults
  – Example: a CPU halts (for any reason) and a defect in recovery code in another CPU induces another halt

• Therefore, masking of single halts is beneficial even when the application is fault tolerant
  – Reduces the opportunities for having an outage

• DMR and TMR mask single hardware failures
• S series and NSVA do not
Impact of Repairing a CPU

• S series:
  – Loss of the logical processor

• NSVA:
  – Loss of the logical processor

• DMR:
  – No loss of logical processor(s)
  – Loss of fault tolerance and guaranteed data integrity for all logical processors in that blade complex

• TMR:
  – No loss of logical processor(s)
  – No loss of fault tolerance for any logical processors in that blade complex